Buffer Transport Mechanisms in Intentionally Carbon Doped GaN Heterojunction Field Effect Transistors

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Abstract

Temperature dependent pulsed and ramped substrate bias measurements are used to develop a detailed understanding of the vertical carrier transport in the buffer layers in a carbon doped GaN power heterojunction field effect transistor. Carbon doped GaN and multiple layers of AlGaN alloy are used in these devices to deliver an insulating and strain relieved buffer with high breakdown voltage capability. However, understanding of the detailed physical mechanism for its operation is still lacking. At the lowest electric fields (< 10MV/m), charge redistribution within the C doped layer is shown to occur by hole conduction in the valence band with activation energy 0.86eV. At higher fields, leakage between the two-dimensional electron gas and the buffer dominates occurring by a Poole-Frenkel mechanism with activation energy ~0.65eV, presumably along threading dislocations. At higher fields still, the strain relief buffer starts to conduct by a field dependent process. Balancing the onset of these leakage mechanisms is essential to allow the build-up of positive rather than negative space charge, and thus minimize bulk-related current-collapse in these devices.

GaN based Heterojunction Field Effect Transistors (HFET) are being actively developed for high power, high voltage switching applications. The increased power density compared to conventional silicon devices arises from a combination of high electron mobility and high breakdown voltage. However there remain challenges associated with the control of device leakage and in particular current-collapse (CC) or dynamic on-resistance [1]. CC is a result of slow, reversible, negative charge storage during the OFF state of the switching transistor affecting the ON state conduction. Power GaN HFETs are grown on silicon substrates of 6" or 8" diameter, therefore epitaxial growth requires strain relief layers, typically graded or superlattice AlGaN based, to control wafer bow resulting from lattice and thermal expansion mismatch. On top of these layers, a semi-insulating GaN layer is required before the final AlGaN barrier layer which induces the active two dimensional electron gas (2DEG). In this paper, we analyze the impact of carbon doping of the GaN on transport mechanisms. Carbon results in the Fermi level being pinned about 0.9eV above the valence band [2, 3] and is the most commonly used dopant for GaN power devices delivering excellent control of leakage with high breakdown voltage, but can also be associated with CC[1, 4]. Device modelling has predicted that this C doping would result in a floating weakly p-type layer, with dramatic CC far exceeding what is normally measured[5]. Using substrate biased measurements, it has recently been shown that a band-to-band leakage path, presumably via trap-assisted-tunneling (TAT) along threading dislocations, can transport electrons from the floating C-doped buffer to the two dimensional electron gas (2DEG) largely suppressing the current-collapse[6, 7]. However the detailed mechanism of the charge transport in this buffer is lacking. Here we develop a detailed physical understanding of the different transport mechanisms within the buffer of a C-doped GaN power HFET, show how those mechanisms affect the ability of the buffer to store charge, and relate those mechanisms to the susceptibility of the transistors to CC.

Ungated Ohmic structures fabricated using a GaN HFET process targeted at 600V operation were studied. Two different epitaxial layer structures were considered consisting of GaN capped AlGaN barrier, a 1.5µm GaN layer comprising an undoped channel region above a compensated heavily

carbon doped layer, strain relief layers of thickness either 1.4µm (Wafer A) or 3.3µm (Wafer B), on a p-type silicon substrate. The device structures had gaps of 5 to 60µm between the Ohmic contacts containing a 2DEG of sheet resistance ~700 Ω/square. Example transistor characteristics from this process development can be seen in [8] and had a pinch-off voltage of -2V. More details on similar devices are given in [6].

To gain insight into the transport in the C-doped GaN buffer layer, the change in conductivity of the 2DEG in the contact gaps was used to monitor changes in the vertical electric field in the buffer below the 2DEG. Changes in the conductivity can then be used to quantify bulk charge storage and trapping. The key advantage of this approach,[9,6, 10, 11] is that surface effects and trapping are excluded, allowing unambiguous measurement of buffer trapping alone. Only negative substrate bias, V_{SUB}, is considered here since this corresponds to the polarity experienced by a transistor under OFF state conditions. The time dependence of the 2DEG conductivity was measured following the application of a substrate bias as a function of temperature.

At the lowest voltages, an average field of <10MV/m, a small negative going conductivity transient of magnitude up to a few % was observed as can be seen in Fig. 1, whereas at larger voltage this was overlaid by a positive going transient of magnitude up to about 30% as illustrated in Fig. 2. The negative transient corresponds to an increase in vertical field under the 2DEG and hence negative charge storage in the bulk, whereas the positive transient corresponds to a decrease in field and hence positive charge storage. Measuring the transient time constants between 40°C and 150°C allowed activation energies to be extracted, as shown in the inset to Fig. 2. The negative transient had an activation energy of 0.86eV, and the positive transient showed an activation energy of 0.7eV at low fields which decreased with increasing vertical electric field at the same rate in both wafers.

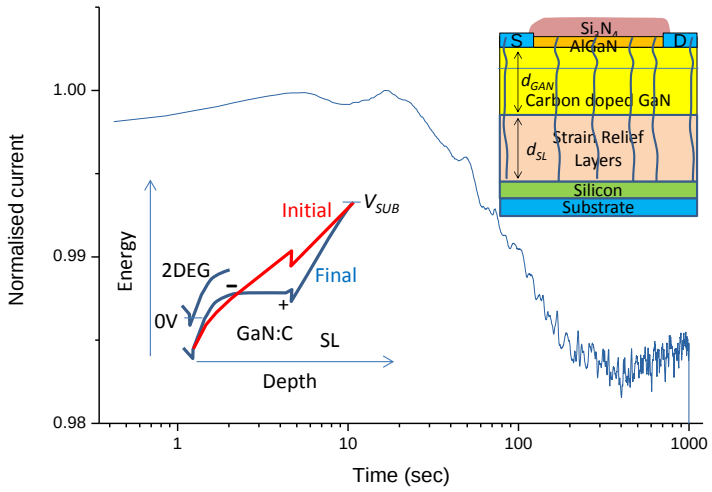

Figure 1. Normalised current transient in 60µm wide contact gap on Wafer A at 130°C with gap-bias of 1V following a step in the substrate bias, V_{SUB}, from 0V to -25V (9MV/m). The insets shows the device structure with threading dislocations, and a schematic band diagram immediately after applying V_{SUB} and then after reaching equilibrium.

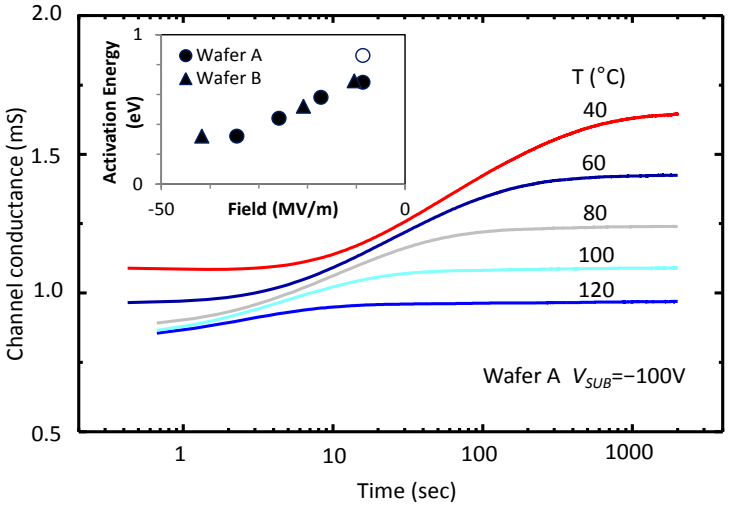

Figure 2. Current transient in 60µm contact gap on Wafer A with an applied bias of 1V following a step in V_{SUB} from 0V to -100V (34MV/m) at different temperatures. The inset shows the inferred activation energy for the transient time constant vs initial average field. Open symbol is for the negative going transient and the closed symbols are for the positive transients.

To help understand this behavior and demonstrate that the apparent decrease in activation energy with increasing bias for the positive transient was in fact due to a transition between two conduction mechanisms, complementary measurements were undertaken by ramping the substrate bias. Varying the ramprate generates a capacitive displacement current which allows vertical

transport to be probed in the regime where vertical leakage is very small, in this case up to about 100MV/m. Figure 3 shows the normalized 2DEG current at varying ramp rate. Initially the 2DEG current decreased linearly with V_{SUB}, at a rate consistent with the entire buffer stack acting as an insulating dielectric, however it then saturated at voltages above $|V_1|$ before starting to decrease again above $|V_2|$. The saturation implied that the field under the 2DEG had become bias independent, in turn implying positive charge accumulation below the 2DEG [6]. At voltage V_2, the stored positive charge stopped increasing as another transport mechanism turned on. Saturation in current between V_1 and V_2 occurred when the hole leakage into the buffer equaled the vertical displacement current $J=CdV/dt$ allowing positive charge to accumulate. Hence a J-V characteristic for the vertical leakage paths can be constructed by measuring the saturation voltages at varying displacement current. Fig. 4 shows the current dependence of the characteristic voltages V_1 and V_2 demonstrating strongly temperature dependent non-Ohmic conduction. In the wafers measured here, there was only a small variation in the normalized change in current as the contact gap was increased. This implied that lateral conduction in the layers on a length scale of microns was insignificant compared to vertical conduction (in contrast to the sample discussed in Ref. [6]).

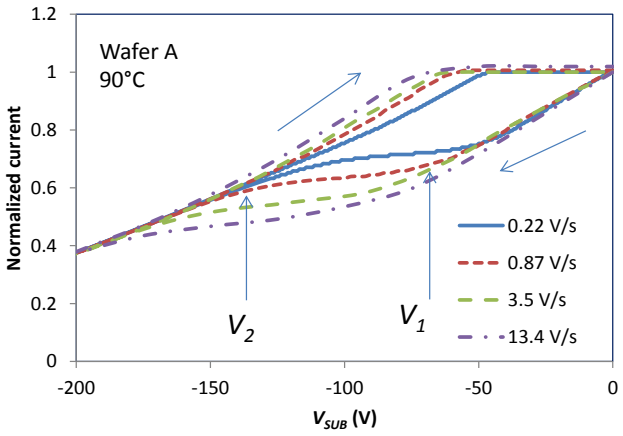

Figure 3. Normalised current in 60µm contact gap in Wafer A with an applied bias of 1V as V_{SUB} is ramped from 0V to -200V to 0V at the indicated ramp rates. V_1 and V_2 indicate the start and end of the current saturation during the down ramp.

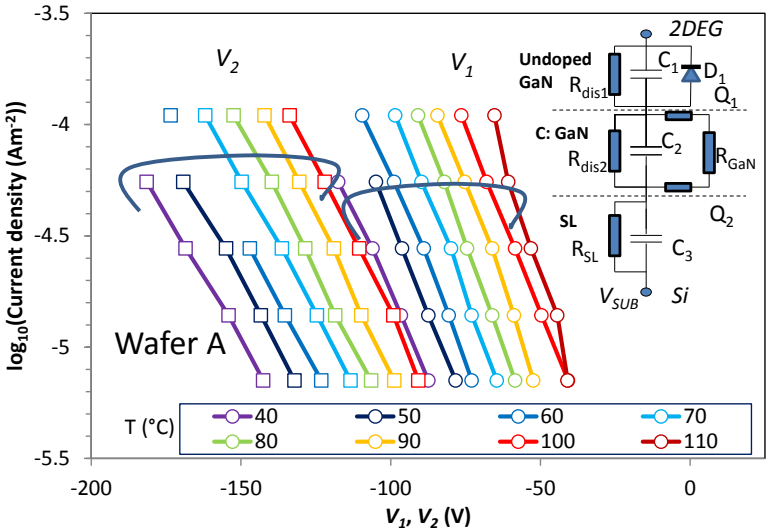

Figure 4. Current density J versus V_1 and V_2 at different temperatures. The inset shows the buffer lumped equivalent circuit.

GaN grown on Si is highly defective typically containing 10^9 to 10^{10}cm^{-2} threading dislocations. Work on GaN based light emitting diodes (LEDs) has clearly demonstrated that leakage across reverse biased junctions is linked to the density of screw and mixed dislocations[12, 13, 14]. In LEDs rather than observing an activation energy corresponding to either full or half bandgap, a highly non-Ohmic leakage path has been seen corresponding to either variable range hopping or Poole-Frenkel conduction with activation energy as low as 130meV. This band-to-band leakage has been linked to a TAT mechanism via a high density of defect levels located throughout the bandgap[15]. For the power HFET structure of the inset to Fig. 1, this mechanism would allow the injection of holes originating from the 2DEG into the p-type C-doped GaN buffer under negative V_{SUB} conditions. Although the LED has indium containing alloys and Mg p-type dopant, it nevertheless seems likely that dislocations in unintentionally or C-doped GaN are also electrically active under high field conditions[6].

To help interpret the ramped and transient measurements, a lumped equivalent circuit representation was used as shown in the inset to Fig. 4, where the 2DEG density senses the voltage drop across the diode D_1. Here we have represented the non-linear conduction in the threading

dislocations in the undoped and C-doped GaN by R_{dis1} and R_{dis2}, the C-doped GaN by R_{GaN}, and the strain relief buffer by R_{SL}. Forward bias of the 2DEG to p-type buffer is captured by D_1 when electrons are readily injected into the buffer cancelling any stored positive charge, and which is clearly observed in Fig. 3 as current saturation as the reverse sweep approaches 0V.

Considering first the small negative transient observed at low biases (Figure 1), the activation energy of 0.86eV is entirely consistent with conduction by activation to the valence band edge from C acceptors[3]. If we assume that at this low field of <10MV/m the conductivity of the strain relief layer, the dislocations, and the undoped region are insignificant, then the sign of the conduction change can be explained by a slow redistribution of charge by hole conduction resulting in the dipole shown in the inset to Fig. 1, and corresponding to Q_1=-Q_2. Assuming that an equipotential in the C doped GaN was achieved at long times, then electrostatics predicts a transient magnitude of ~5% for V_{SUB}=−25V in Wafer A. This is consistent with the 2% change seen in Fig. 1.

As the vertical field increases (corresponding to >|V_1| or 10-30MV/m in Figure 3), the dislocations start to conduct from the 2DEG allowing positive charge to accumulate in the C-doped GaN layer as charge Q_2, and replacing the negative transient with a positive transient. Taking the *J*-V_1 data in Fig. 4 and replotting it in Fig. 5, it is found to be consistent with a Poole-Frenkel mechanism of the form

$$J/E \propto exp\left[\frac{-q(\phi_B-\sqrt{qE/\pi\epsilon})}{k_BT}\right] \quad (1)$$

where ε is the dielectric constant, and ϕ_B the trap energy[16]. The electric field *E* was estimated assuming a uniform field between the 2DEG and the Si substrate which will overestimate the field as a result of the accumulation of charge within the GaN during the ramp. Fig. 5 shows that there is excellent consistency between the two thicknesses of wafer demonstrating that the mechanism scales with electric field. The trap energy was found to be about 0.65eV in both wafers consistent with the low field measurements in Fig. 2. The electric field induced barrier lowering (as shown in

the inset to Fig. 5) decreased about twice as fast as expected from equation (1), likely as a result of the electric field overestimate. All this suggests that Poole-Frenkel conduction in the GaN layer, presumably along the dislocations, is indeed occurring at fields >10MV/m. In these samples the data was not consistent with space charge limited conduction[10].

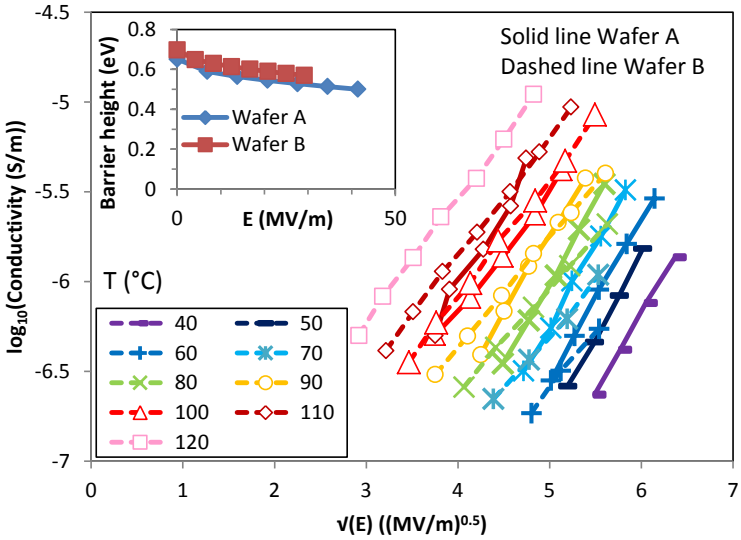

Figure 5. Conductivity of the dislocations from 2DEG to C-doped GaN versus root electric field, considering Poole-Frenkel conduction for wafer A and B at different temperatures. The inset shows the inferred barrier height as a function of vertical electric field.

At voltages above $|V_2|$ in Fig. 3, the strain relief layers start to conduct resulting in the positive charge Q_2 in the C-doped buffer being partially neutralized by conduction from the Si, although it cannot be determined whether this occurs by hole transport from the C-doped GaN to the Si or by electron injection from the Si layer. The inset to Figure 6 shows how the band bending varies through the structure between V_1 and V_2, as positive charge Q_2 screens the electric field under the 2DEG keeping the potential at the bottom of the GaN layer constant at voltage V'. Hence the electric field in the strain relief layer at V_2 will be approximately $E_2=V_2/d_{SL}-V_1 d_{GaN}/[d_{SL}(d_{GaN}+d_{SL})]$. In this case the resulting current versus field data was not sufficient for an unambiguous extraction of the conduction mechanism, with both Poole-Frenkel and Schottky emission producing a reasonable fit. Nevertheless it seems plausible that the leakage is associated with Poole-Frenkel conduction along the dislocations in the wider bandgap strain relief layers. Fig. 6 shows a Poole-Frenkel plot

where the similar field dependence in both wafers, and the higher onset field of ~40MV/m, are consistent with that model.

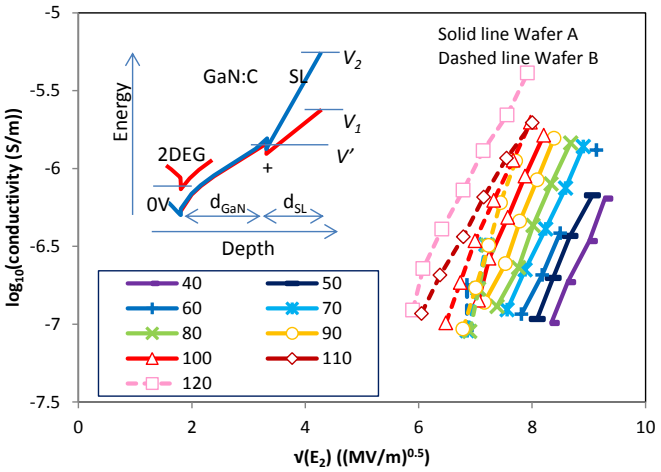

Figure 6. Conductivity of the strain relief layers versus root electric field in the strain relief layer, considering Poole-Frenkel conduction for wafers A and B at different temperatures. The inset shows the band bending at $V_{SUB}=V_1$ and V_2.

In these wafers, leakage through the top part of the structure (GaN layer) occurs at lower fields than in the strain relief layers at the bottom, resulting in the accumulation of a net positive charge in the buffer (as ionized compensating donors or possibly free holes). A key point is that positive charge stored during the OFF state of a C-doped GaN HFET can be quickly neutralized by injection of electrons from the 2DEG when switched to the ON-state, potentially delivering good CC performance. In the absence of such a leakage path, or where lateral leakage in the C doped p-type layer is dominant, a reverse biased negatively charged depletion region can form under the drain resulting in a high drain resistance and poor CC [5, 7]. Here we have considered largely one-dimensional transport whereas CC is a complex dynamic two-dimensional problem involving both positive and negative stored charge in different parts of the HFET[5]. However it is clear that understanding and designing the buffer for minimum CC requires full control of all the leakage paths and blocking layers in addition to controlling the defect and dopant densities.

In summary, temperature and substrate bias dependent measurements have been undertaken to determine the vertical transport mechanisms in the epitaxy used for a power GaN HFET. In the bias regime well below breakdown, it is found that a complex vertical transport process is operative. At low fields, the C-doped GaN layer is effectively isolated from the 2DEG and hole conduction and charge redistribution has been observed with an activation energy of 0.86eV consistent with the carbon acceptor level. However the most important contribution to the transport arises from non-Ohmic conduction presumably along threading dislocations at fields above 10MV/m. In the GaN, holes originating in the 2DEG flow into the GaN buffer by a Poole-Frenkel mechanism with activation energy ~0.65eV. This stored positive charge reduces the field under the drain and reduces susceptibility to current-collapse. At fields >40MV/m the strain relief buffer starts to conduct by a field driven process, limiting the positive charge which can be stored in the C-doped buffer.

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